ABSTRACT OF THE DISCLOSURE

The read speed of an on-chip nonvolatile memory enabling electric rewrite is increased. The nonvolatile memory has a hierarchal bit line structure having first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the plurality of memory arrays, a first selector circuit selecting the first bit line for each of the memory arrays to connect the selected first bit line to the second bit line, and a sense amp arranged between the output of the first selector circuit and the second bit line. The hierarchal bit line structure having the divided memory arrays can reduce the input load capacity of the sense amp.